# Notice of References Cited

Application/Control No. 10/080,823

Applicant(s)/Patent Under Reexamination HINO ET AL.

Examiner Phallaka Kik Art Unit 2825

Page 1 of 2

# U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,008,821	12-1999	Bright et al.	345/504
	В	US-5,757,654	05-1998	Appel, William Dale	716/1
	С	US-5,488,583	01-1996	Ong et al.	365/201
	D	US-6,470,475	10-2002	Dubey, Prashant	716/1
	Е	US-6,304,241	10-2001	Udo et al.	345/96
	F	US-4,214,269	07-1980	Parker et al.	348/442
	G	US-6,256,604	07-2001	Yabe et al.	703/14
	Н	US-4,833,620	05-1989	Takahashi, Hitoshi	716/4
	1	US-4,447,881	05-1984	Brantingham et al.	716/17
	J	US-			
	К	US-			
	L	US-	,		
	М	US-			

## FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP 10256512 A	09-1998	Japan	KAJITANI et al.	H01L 27/108
	0	JP 07211075 A	08-1995	Japan	AKIYAMA et al.	G11C 11/41
	Р	JP 02183558 A	07-1990	Japan	HIROKI, MASANORI	H01L 27/04
	Q	JP 02078268 A	03-1990	Japan	KUBODERA et al.	H01L 27/10
	R	JP 02005292 A	01-1990	Japan	OHATA et al.	G11C 11/41
	s	JP 63209141 A	08-1988	Japan	URASAKI, TADAAKI	H01L 21/82
	Т	JP 11086531 A	03-1999	Japan	HASEGAWA et al.	G11C 11/401

### **NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	NB8909290, "Method to Improve Chip Wiring", IBM Technical Disclosure Bulletin, Vol. 32, No. 4B, September 1989, pp. 290-293 (6 pages).
	٧	Nakamura et al., "A 29-ns 64-Mb DRAM With Hierarchical Array Archictecture", IEEE Journal of Solid-State Circuits, Vol. 31, N 9, September 1996, pp. 1302-1307.
	w	Wada et al., "Varialbe Bit Organization as a New Test Function for Standard Memories", IEEE Journal of Solid-State Circuits, Vol. 26, No. 1, January 1991, pp. 51-54.
	х	Mulder et al., "An Area Model for On-Chip Memories and its Application", IEEE Journal of Solid-State Circuits, Vol. 26, No. 2, February 1991, pp. 98-106.

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

# Application/Control No. 10/080,823 Applicant(s)/Patent Under Reexamination HINO ET AL. Examiner Phallaka Kik Page 2 of 2

### **U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-			
	В	US-			
	С	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	Ι	US-			
	_	US-			
	J	US-			***
	К	US-			
	L	US-			
	М	US-			

## FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	WO 9858410 A1	12-1998	World Intellect	KITSUKAWA et al.	H01L 27/10
	0	JP 11154708 A	06-1999	Japan	SERA, YOSHIAKI	H01L 21/82
	Р	JP 11068059 A	03-1999	Japan	FUJISAWA, HIROKI	H01L 27/108
	Q	JP 11054726 A	02-1999	Japan	SUZUKI et al.	H01L 27/108
	R	JP 04144276 A	05-1992	Japan	KIKUTA et al.	H01L 27/10
	s					
	T					

### **NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	w	
	х	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.